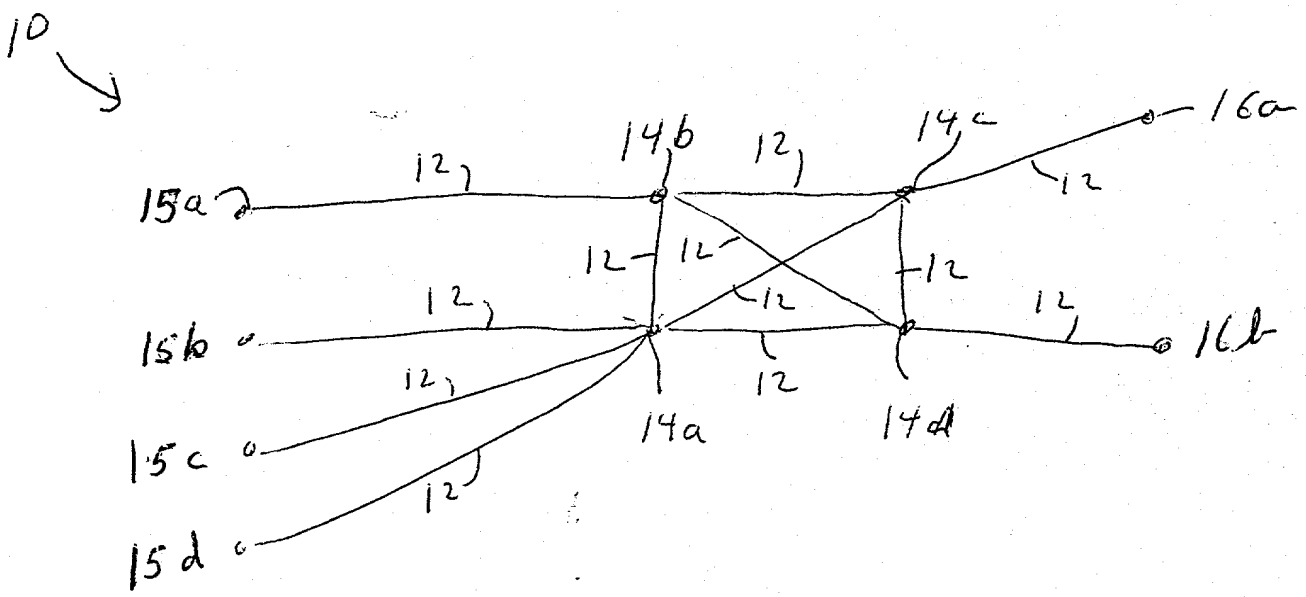

Fig. 1

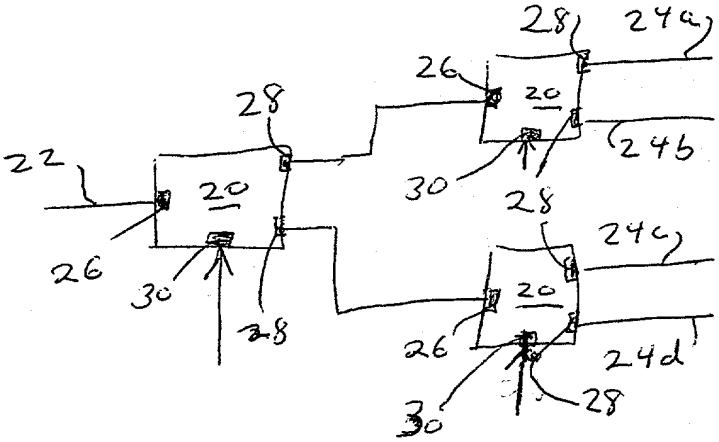

Fig. 2

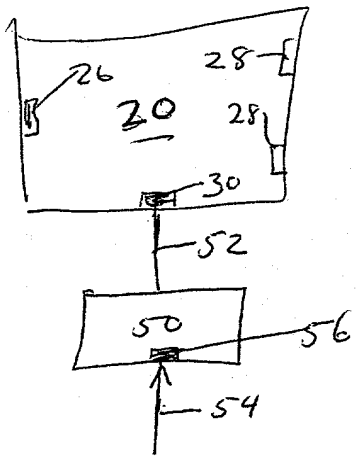

Fig. 3

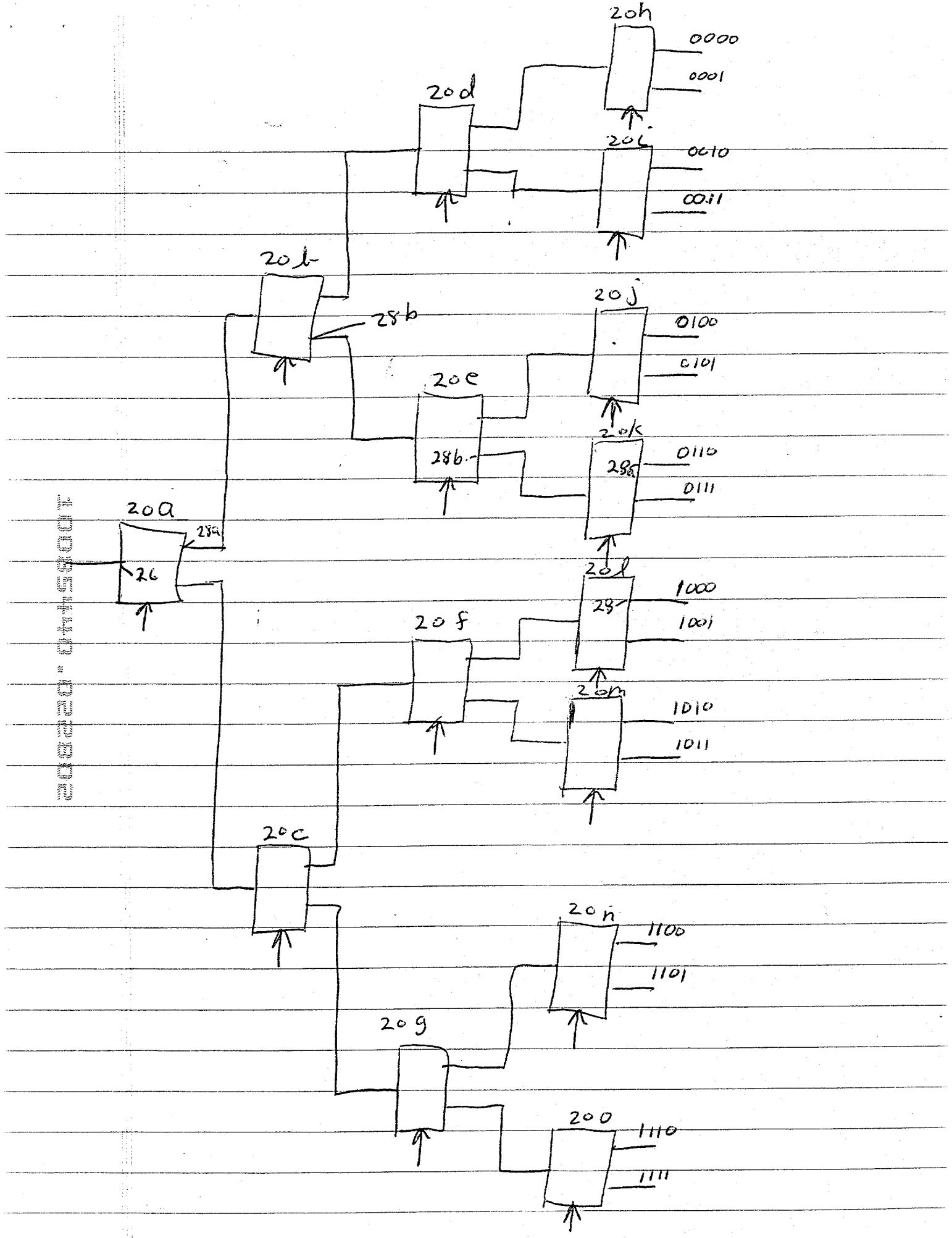
20h
0000
0001
20d
20i
0010
0011
20b
28b
20j
0100
0101
20e
20k
28b
28a
0110
0111
20a
28a
26
20l
28
1000
1001
20f
20m
1010
1011
20c
20n
1100
1101
20g
200
1110
1111

Figure 4

	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	
0000	1	1	x	1	x	x	x	1	x	x	x	x	x	x	x	
0001	1	1	x	1	x	x	x	0	x	x	x	x	x	x	x	
0010	1	1	x	0	x	x	x	x	1	x	x	x	x	x	x	
0011	1	1	x	0	x	x	x	x	0	x	x	x	x	x	x	
0100	1	0	x	x	1	x	x	x	x	1	x	x	x	x	x	
0101	1	0	x	x	1	x	x	x	x	0	x	x	x	x	x	
0110	1	0	x	x	0	x	x	x	x	x	1	x	x	x	x	← 54
0111	1	0	x	x	0	x	x	x	x	x	0	x	x	x	x	
1000	0	x	1	x	x	1	x	x	x	x	x	1	x	x	x	
1001	0	x	1	x	x	1	x	x	x	x	x	0	x	x	x	
1010	0	x	1	x	x	0	x	x	x	x	x	x	1	x	x	
1011	0	x	1	x	x	0	x	x	x	x	x	x	0	x	x	
1100	0	x	0	x	x	x	1	x	x	x	x	x	x	1	x	
1101	0	x	0	x	x	x	1	x	x	x	x	x	x	0	x	
1110	0	x	0	x	x	x	0	x	x	x	x	x	x	x	1	
1111	0	x	0	x	x	x	0	x	x	x	x	x	x	x	0	

"1" - top port
"0" - bottom port
"x" - "don't care"

Figure 5

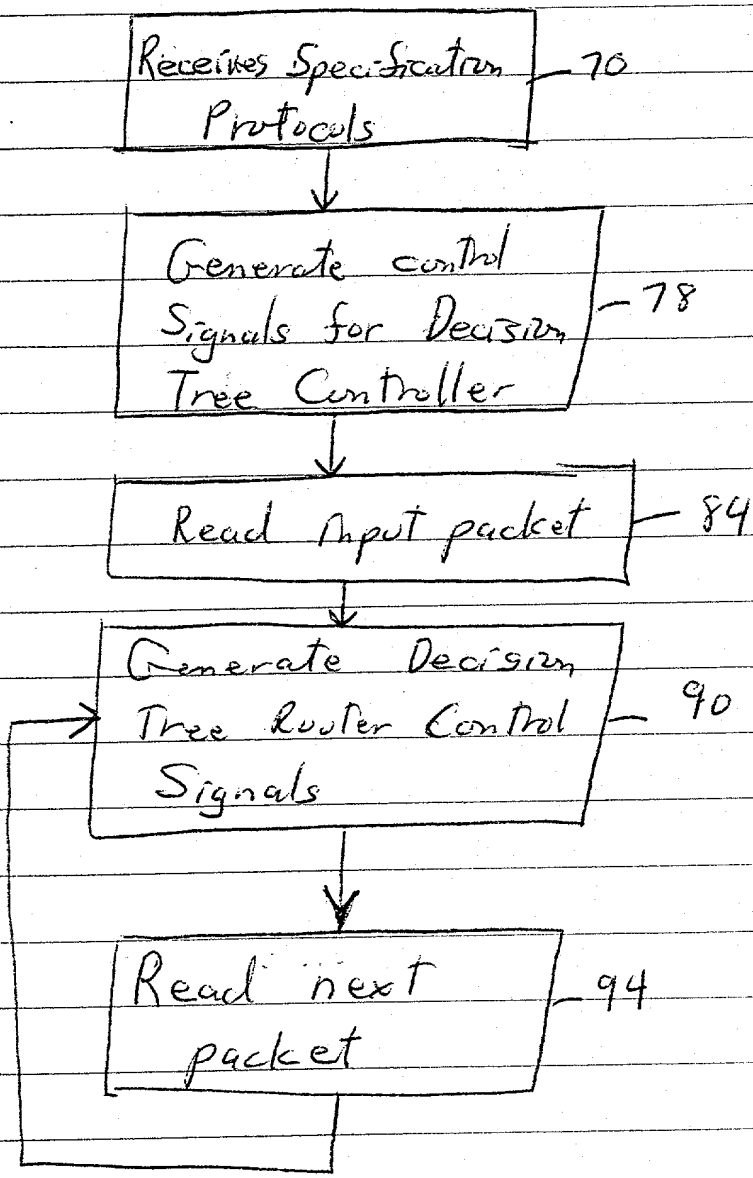
Receives Specification Protocols
70
Generate control Signals for Decision Tree Controller
78
Read Input packet
84
Generate Decision Tree Router Control Signals
90
Read next packet
94

Fig 6

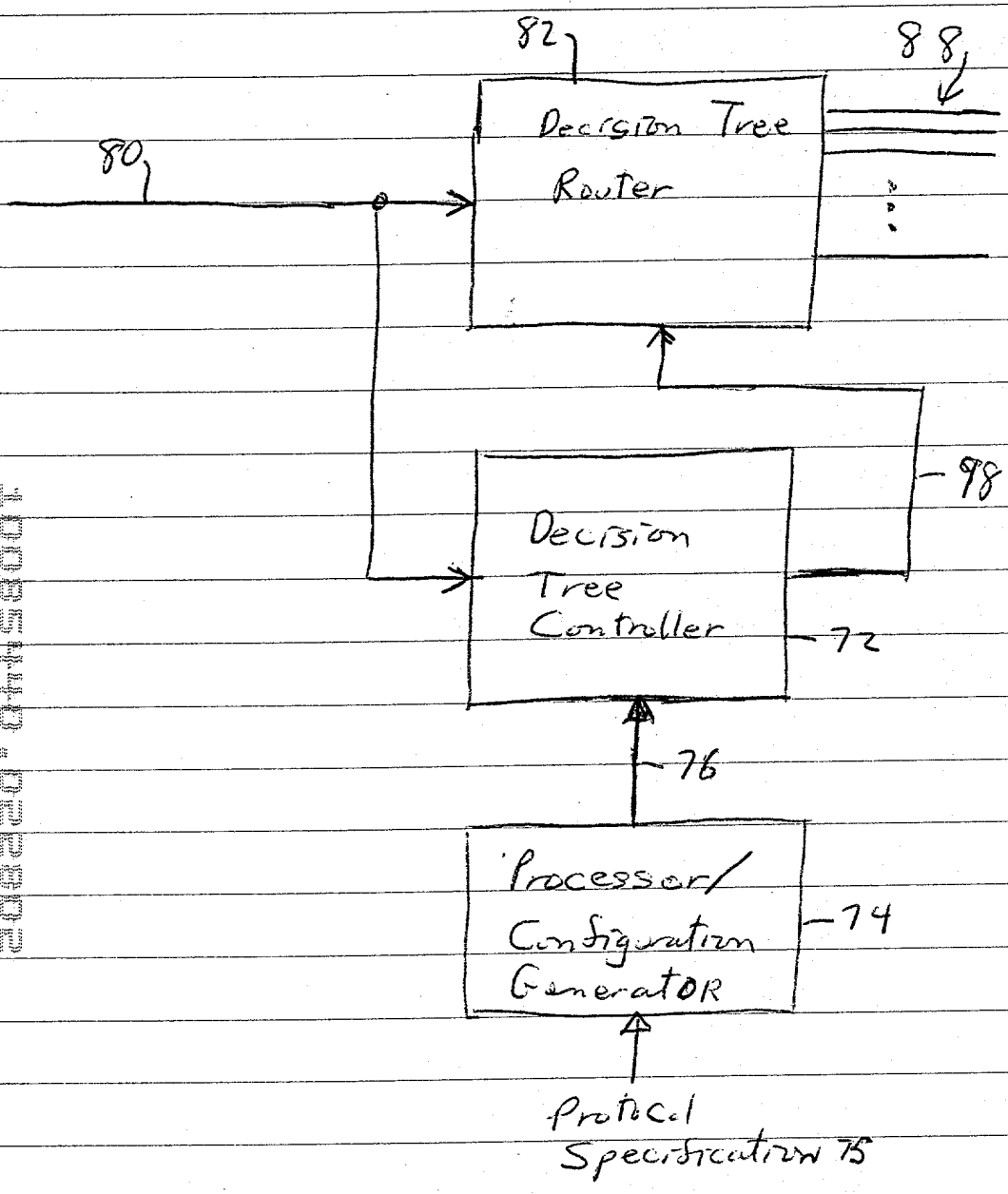
82
88
Decision Tree
Router
80
98
Decision
Tree
Controller
72
76
Processor/
Configuration
Generator
74
Protocol
Specification 75

Fig. 7